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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,401	07/10/2002	Emily E. Fisch	BUR920010180	7447

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SCHMEISER, OLSEN + WATTS
SUITE 201
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LATHAM, NY 12033

EXAMINER	
ROSASCO, STEPHEN D	

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,401	FISCH ET AL.	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/10/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Tong et al. (6,352,803) or Ghandehari et al. (6,589,717).

The applicant discusses the limitations of the prior art in that during fabrication of an extreme ultraviolet lithography (EUVL) mask structure, defects in the EUVL mask structure are inadvertently generated. Unfortunately, repair of such defects by use of, inter alia, a charged particle beam, a laser beam, etc. may modify the EUVL mask in a manner that impairs the effectiveness of the EUVL mask. Thus, there is a need for a structure and associated method that enables EUVL mask defects to be repaired without impairing the effectiveness of the EUVL mask.

The claimed invention is directed to an extreme ultraviolet lithography (EUVL) mask structure, and a method of forming comprising: providing a first conductive layer between a buffer layer and an absorber layer such that the buffer layer is on a multilayer stack that is adapted to substantially reflect EUV radiation incident thereon, and wherein the absorber layer is adapted to absorb essentially all of EUV radiation incident thereon;

forming a mask pattern in the absorber layer accompanied by inadvertent formation of a defect in the absorber layer; and repairing the defect.

And wherein repairing the defect includes directing a beam of charged particles into the absorber layer and toward the first conductive layer, and wherein the first conductive layer shields the buffer layer from electric charge accumulation.

Tong et al. teach a process for creating a mask substrate involving depositing: 1) a coating on one or both sides of a low thermal expansion material EUVL mask substrate to improve defect inspection, surface finishing, and defect levels; and 2) a high dielectric coating, on the backside to facilitate electrostatic chucking and to correct for any bowing caused by the stress imbalance imparted by either other deposited coatings or the multilayer coating of the mask substrate. A film, such as TaSi, may be deposited on the front side and/or back of the low thermal expansion material before the material coating to balance the stress. The low thermal expansion material with a silicon overlayer and a silicon and/or other conductive underlayer enables improved defect inspection and stress balancing.

In FIG. 2, the EUVL mask substrate 20 comprises a substrate 11, multilayers 12, buffer layer 13, and an absorber pattern 14, as in FIG. 1, but with an addition of a front coating 21 located between substrate 11 and multilayers 12 to enhance defect inspection, balance stress, smooth defects, and/or be repolished. The front coating 21 is composed of material such as Si, Mo, Cr, chromium oxynitride, TaSi, or Mo/Si multilayers.

Ghandehari et al. a mask blank used for EUV lithography, which can be a reflecting mask constructed from a Si wafer over which a multilayer mirror is constructed from alternating layers of Si and Mo. On the surface of the multilayer, a buffer layer of 500 ANG SiOsub2 is made to allow for defect repair and etch protection during feature patterning. Above the buffer layer, the features are normally deposited and patterned. After the features on the mask are patterned, the SiOsub2 layer is etched in areas other than the features to reveal the multi-mirror surface.

FIG. 3 illustrates a portion 30 of an integrated circuit including a substrate 32, a multilayer mirror 34, a buffer layer 36, an aluminum layer 38, and a hard mask 40. In an exemplary embodiment, hard mask 40 is a Ni hard mask which is grown selectively by photon assisted CVD. Multilayer mirror layer 34 can be constructed from alternating layers of silicon (Si) and molybdenum (Mo). In an exemplary embodiment, there are 40 layers in multilayer mirror in total with each silicon (Si) layer being 4 nm while the molybdenum (Mo) layers are 3 nm. The 40 layers gives a mask blank with 65-70% reflectivity to the 13.4 nm EUV radiation.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tong et al. (6,352,803) or Ghandehari et al. (6,589,717).

The description of the invention and cited art is included here from before.

The teachings of Tong et al. or Ghandehari et al. differ from those of the applicant in that the applicant teaches the use of a second conductive layer and some variations in the arrangements of the different layers. However, these modifications would be determined more by design specifications. Therfore, it would have been obvious to one having ordinary skill in the art to take the teachings of Tong et al. or Ghandehari et al. and change the order of layers on the substrate or add a second conductive layer in order to make the claimed invention because for the most part the layers function independently, while the conductive layer is utilized to prevent damage to the mask resulting from the repair processes and the use of a

second conductive layer would be dictated by the extent of conductivity needed to neutralize the impact of the particular repair technique.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Rosasco whose telephone number is 571-272-1389. The examiner can normally be reached on M-F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff, can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

For general Information call (571-272-1700).

S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
2/11/04